

10/727474

LSI LOGIC

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From: **Name:** Manu Kashyap, Intellectual Property Paralegal
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Telephone: (408) 433-7475
Fax: (408) 433-7460
Re: 6,954,082

Number of Pages Including this Page 4

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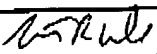
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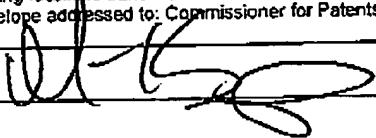
TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	6,954,082 B2
	Filing Date	October 11, 2005
	First Named Inventor	Carlo Grilletto
	Art Unit	2829
	Examiner Name	Nguyen, Tu
	Attorney Docket Number	03-1681
Total Number of Pages in This Submission		3

ENCLOSURES (Check all that apply)		
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Firm Name	LSI Logic Corporation		
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Printed name	Timothy Croll		
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(Also Form PTO-1050)**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1PATENT NO. : 6,954,082 B2

APPLICATION NO.: 10/727,474

ISSUE DATE : October 11, 2005

INVENTOR(S) : Carlo Grilletto

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page at column 12, please delete "Grillettc" and replace with - Grilletto -

On the cover page at column 75, please delete "Grillettc" and replace with - Grilletto -

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Should be "Grilletto"



US006954082B2

(12) **United States Patent**
Grilletto

(10) Patent No.: **US 6,954,082 B2**
(45) Date of Patent: **Oct. 11, 2005**

Should Be
"Grilletto"

(54) **METHOD AND APPARATUS FOR TESTING OF INTEGRATED CIRCUIT PACKAGE**

(75) Inventor: Carlo Grilletto, San Carlos, CA (US)

(73) Assignee: LSI Logic Corporation, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/727,474

(22) Filed: Dec. 4, 2003

(65) Prior Publication Data

US 2005/0122127 A1 Jun. 9, 2005

(51) Int. Cl. G01R 31/26

(52) U.S. Cl. 324/765

(58) Field of Search 324/760, 754, 324/755, 757, 765, 158.1, 761, 763

(56) References Cited

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* cited by examiner

Primary Examiner—Vinh Nguyen

Assistant Examiner—Tung X. Nguyen

(74) Attorney, Agent, or Firm—L. Jon Lindsay

(57) ABSTRACT

A method and apparatus for testing an integrated circuit (IC) package includes a printed circuit board (PCB) on which is mounted the IC package and which is removably connected (preferably perpendicular) to a motherboard. The IC package, the PCB and the motherboard are subjected to thermal, humidity and/or electrical test conditions.

20 Claims, 4 Drawing Sheets

